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Work Function Modulation and Thermal Stability of Reduced Graphene Oxide Gate Electrodes in MOS Devices

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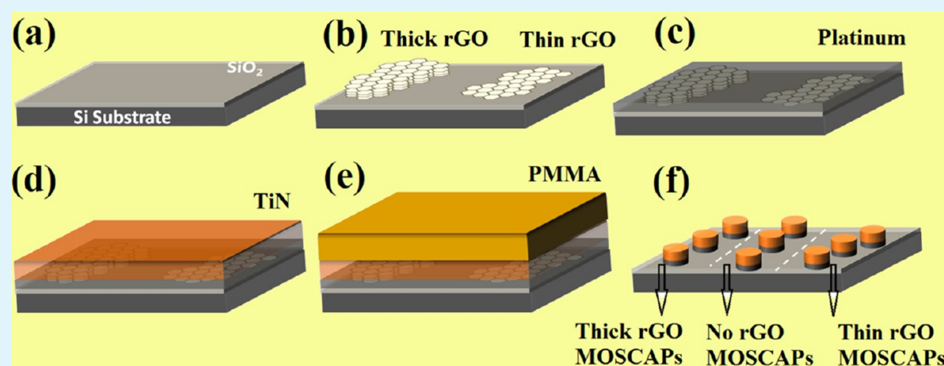
Supporting Information



ABSTRACT: Work function (WF) tuning of the contact electrodes is a key requirement in several device technologies, including organic photovoltaics (OPVs), organic light-emitting diodes (OLEDs), and complementary metal oxide semiconductor (CMOS) transistors. Here, we demonstrate that the WF of the gate electrode in an MOS structure can be modulated from 4.35 eV (n-type metal) to 5.28 eV (p-type metal) by sandwiching different thicknesses of reduced graphene oxide (rGO) layers between top contact metals and gate dielectric SiO_2. The WF of the gate electrode shows strong dependence on the rGO thickness and is seen to be nearly independent of the contact metals used. The observed WF modulation is attributed to the different amounts of oxygen concentrations in different thicknesses of rGO layers. Importantly, this oxygen concentration can also be varied by the reduction extent of the graphene oxide as experimentally demonstrated. The results are verified by X-ray photoelectron spectroscopy and Fourier transform infrared spectroscopy analyses. The obtained WF values are thermally stable up to 800 °C. At further high temperatures, diffusion of metal through the rGO sheets is the main cause for WF instability, as confirmed by cross-sectional high-resolution transmission electron microscopy analysis. These findings are not limited to MOS devices, and the WF modulation technique has the potential for applications in other technologies such as OLEDs and OPVs involving graphene as conducting electrodes.

KEYWORDS: *graphene, reduced graphene oxide, work function tuning, CMOS, thermal stability, dielectric reliability, Fourier transform infrared spectroscopy*

INTRODUCTION

Significant efforts have been made to utilize the spectacular material properties of monolayer graphene (Gr) for a variety of applications. One of the most discussed domain of graphene's applications is in electronics due to its exceptionally high carrier mobility, thermal stability, mechanical flexibility, and atomically thin two-dimensional sheetlike structure.[1] These properties have been explored in a variety of device applications, e.g., in graphene photodetectors,[2] graphene transistors,[3,4] graphene optical modulators,[5] and graphene conducting electrodes.[6−12] Application of graphene as conducting electrodes is predicted to be its first entry point into the electronic industry as these applications do not require very high quality graphene.[1] Graphene conducting electrodes are being examined for technologies such as touch screens, rollable electronic papers,[1] organic photovoltaics (OPVs),[7,8,10,13] organic field effect transistors,[11,12] and organic light-emitting diodes (OLEDs).[6,9]An important parameter that may affect the performance of these devices is the graphene work function (WF).[6−10] For conducting electrode applications, the WF requirements for the anode and cathode materials are different. In OLEDs and OPVs, where graphene is proposed to be used as the anode as well as the cathode material, the anode should be of high WF material to improve the hole injection efficiency, and the cathode should be of low WF material to collect the electrons effectively.[6−10,13] The high WF value for graphene anodes can be achieved by chemical doping of graphene,[6,14] by the use of high WF oxides as a buffer layer,[7] by oxygen plasma

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treatment,[15] or by ozone/ultraviolet treatment,[16] whereas, for graphene cathodes, low WF is reported by combining graphene with an ionic polymer layer for interfacial dipole creation,[8] by nitrogen doping in graphene,[9] by contact doping,[17] or by combining graphene with alkali metal carbonates.[18]

The other important area of the electronic industry is the CMOS technology where similar dual WF values of the gate electrodes are required. The International Technology Roadmap for Semiconductors (ITRS) predicts the need of metals in place of poly-silicon (poly-Si) as a gate electrode in scaled CMOS devices with WF values of metals lying within the range of 0.2 eV of silicon band edges, i.e., 4.0−4.2 eV for NMOS and 5−5.2 eV for PMOS, respectively.[19] With the conventional poly-Si gate electrode, these WF values are achieved by using heavily doped n+ poly-Si and p+ poly-Si for NMOS and PMOS, respectively. With metal electrodes, this can be achieved by using two different metals having low and high WF.[20,21] However, the incorporation of two metals in device processing increases the process complexity[22] and fabrication cost of CMOS technology. Different techniques for modulating the WF of metal gate electrodes have been proposed. Some of them are the following: binary and ternary metal alloys,[23,24] interdiffusion of low and high WF metals at high temperature,[25] implantation of Ar or N_2 into metals,[26] bilayer metal stack,[27] and fully silicided technology.[28,29] With these techniques, the WF can be modulated over a wide range of the silicon band gap. However, some of these techniques suffer from the instability of different metals at high temperatures and a drop in the WF values of different alloys with increasing temperature.[30] In binary and ternary metal alloys, a tight control on the atomic concentration of the different metals is required, whereas, in a fully silicided gate, the control of the silicide phase is a challenge.[29]

A very important virtue of graphene is the dependence of its WF on the graphene thickness.[31] The WF of epitaxial monolayer graphene on SiC is 4.3 eV, which increases to 4.5 eV for four layers and finally saturates to 4.6 eV for higher numbers of layers.[31] These values of the WF are susceptible to change depending on the environment in which graphene is being integrated; e.g., a WF value of 4.5 eV is reported for monolayer graphene on SiO_2, whereas it can be significantly higher at 5.3 eV for monolayer graphene on Al_2O_3.[32,33] These values may further modify when metals of different WFs interact with graphene.[34−37] Different techniques have been employed for the determination of the WF of graphene in the literature.[31,32,38,39] In all of these studies, the basic trend of increasing WF with increasing number of graphene sheets is reported irrespective of the type of graphene and WF measurement techniques. However, the layer-dependent WF tunability of graphene is not explored much for its applications in electronic devices. Dependence of the graphene WF on the number of sheets is an important attribute, which can be utilized in many device applications.

Recently, improved gate dielectric reliability of a MOS device structure with graphene and reduced graphene oxide (rGO) as a gate electrode was demonstrated by Park and Song et al.[33,40,41] and by our group.[42] The studies of refs 33, 40, and 41 are limited to monolayer graphene. We have demonstrated a flat band voltage shift of 0.5 V with reduced graphene oxide (rGO) layers under TiN contact metal in an MOS test structure.[42] However, this flat band voltage shift was only higher with respect to TiN gate electrode devices, and WF tuning was possible in a very narrow range of silicon band gap. Here, we evaluate the WF of rGO with varying thicknesses under different top capping metals (Pt, Ir, Al). We find that very thin rGO (1−3 layers) results in WF values of 4.35 and 4.4 eV with Pt and Ir contact metals, respectively, and a WF of 4.46 eV for Al contact metal. Multilayer rGO (more than 5 layers) results in WF values in the range of 5.16−5.28 eV with these metals. The WF of the gate electrode shows strong dependence on the rGO thickness and increases monotonously from a low value to a high value with increasing rGO thickness under different contact metals. The observed wide range of the WF values cannot be assigned solely to the graphene's layer dependence as the window of thickness-dependent WF for monolayer graphene to multilayer graphene is only from 4.2 to 4.6 eV.[31] In the present work, this wide range of WF modulation is attributed to the different amounts of oxygen concentrations present in the different thicknesses of rGO sheets. This conclusion is well-supported by the physical characterizations such as X-ray photoelectron spectroscopy (XPS) and Fourier transform infrared spectroscopy (FTIR) analyses. This observation is further supported by work function modulation of multilayer rGO by different extents of reduction of graphene oxide (GO). The proposed technique is found to be thermally stable up to 800 °C in nitrogen ambient. Hence, this would be an attractive approach to modulate the work function of MOS gate devices from close to the valence band edge of Si to above the conduction band edge of Si. Other technologies such as OLEDs and OPVs involving graphene as conducting electrodes can also be benefitted by this WF modulation technique.

The rGO used in these experiments is obtained by thermal reduction of graphene oxide (GO). A similar method of thermal reduction of GO into Gr at the device locations was reported earlier.[43] This procedure is suited for MOS technology as GO is easily dispersed in deionized (DI) water, and because of the presence of the negative charge on GO sheets in DI water, they remain well-separated for a long time. Reduced GO and graphene agglomerates in DI water and polar solvents *N*-methylpyrrolidone (NMP) or dimethylformamide (DMF) are used as solvents to avoid agglomeration.[44] However, these chemicals can potentially contaminate the gate dielectric, whereas, on the other hand, DI water is regularly used in CMOS device processing without any detrimental effect on the gate dielectric quality. Graphene obtained by such chemical techniques is known to be of inferior quality in terms of its electron mobility.[1] However, when the material is used as gate electrodes, the electron mobility is not a serious concern, especially when it is capped with a contact metal as described in this work. Graphene synthesized by chemical methods including reduction of graphene oxide are projected to meet the quality requirements for conducting electrode applications.[1] Previously, rGO obtained by different reduction methods has been explored as conducting electrodes in photovoltaics, organic transistors, and light-emitting diodes.[9,13,43,45−48]

■ EXPERIMENTAL SECTION

Materials. Graphene oxide (GO) is prepared by the modified Hummer's method using graphite powder obtained from Sigma-Aldrich. The chemicals $NaNO_3$, H_2SO_4, $KMNO_4$, and H_2O_2 were purchased from Sigma-Aldrich.

Methods. Graphene oxide synthesis and details of device fabrication are given in the Supporting Information.

Characterization. *Physical Characterization.* The thicknesses of the SiO_2 films were measured using a spectroscopic ellipsometer (Sentech, SE 800). To analyze and confirm the thicknesses of rGO

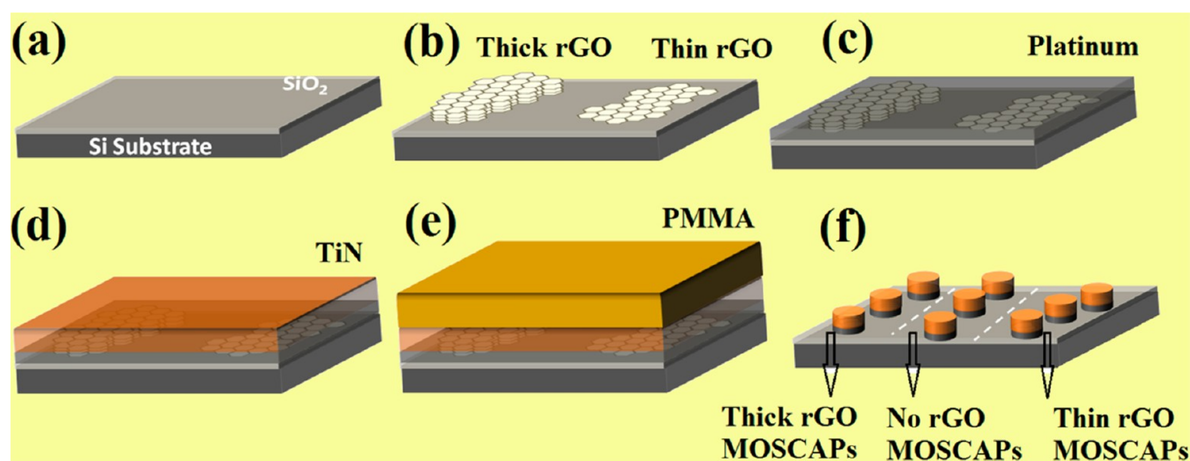

Figure 1. Complete procedure of MOSCAP fabrication with different rGO thicknesses under Pt/TiN contact metal: (a) Starting Si substrate with thermally grown SiO_2. (b) Si/SiO_2 substrate with different thicknesses of rGO after thermal reduction of GO. A region on the same sample is left without rGO for the control sample. Location of the different thicknesses of the rGO is identified in SEM equipped with a lithography technique, and the coordinates are noted for further MOSCAP fabrication. (c, d) Deposition of 20 nm of Pt and 80 nm of TiN as a top capping metal, respectively. (e) PMMA is spin-coated, and the EBL is performed at the already noted positions in step (b). (f) Final top view of as-fabricated MOSCAPs. Regions of the MOSCAPs with different rGO thicknesses are demarked for a better understanding of the procedure.

sheets in the MOS gate stack, cross-sectional high-resolution transmission electron microscopy (HRTEM) analysis of MOS capacitors was performed using a JEOL 2100F instrument. The samples were prepared by mechanical polishing, followed by ion-milling. For TEM sample preparation, the thickness of the Pt metal was reduced to 5 nm as the stack with 20 nm of Pt did not withstand the sample preparation procedure. Ultraviolet photoelectron spectroscopy (UPS) spectra of different rGO thicknesses under Pt metal were collected using a Thermo VG Scientific Multilab 2000 photoelectron spectrometer, which is equipped with a high photon flux He gas discharge source (modes: He I 21.2 eV and He II at 40.8 eV). X-ray photoelectron spectroscopy (XPS) analysis was performed using a MULTILAB from Thermo VG Scientific, equipped with a concentric hemispherical analyzer having a monochromatic Al Kα ($h\nu$ = 1486.6 eV) X-ray source. Peak fitting of the XPS spectra was performed using the software XPS Peak 4.1 (freeware, available at http://xpspeak.software.informer.com/4.1/). Shirley background correction and Gaussian−Lorentzian peak shape was used to fit the peaks. Fourier transform infrared spectroscopy (FTIR) analysis was performed using a Bruker 3000 Hyperion Microscope with a Vertex 80 FTIR system with a spectral resolution of 0.2 cm^{-1}.

Electrical Characterization. MOS capacitors (with and without rGO sheets) were electrically characterized using an Agilent 4284 LCR meter and an Agilent 4156C semiconductor parameter analyzer.

RESULTS AND DISCUSSIONS

MOS capacitors (MOSCAPs) were fabricated on p-type ⟨100⟩ silicon wafers (resistivity ∼ 1−5 Ω cm) with thermally grown SiO_2 of thicknesses of 6.3, 8.5, 10, and 15 nm as the gate dielectric. Varying thicknesses of rGO with different top contact metals (Pt, Ir, Al) were tested as a gate electrode. More details of the rGO preparation and device fabrication procedures are given in the Supporting Information. Extensive use of SEM combined with electron beam lithography ensures the presence of rGO sheets with a fairly good estimation of thickness under different contact metals. Control samples were also fabricated with an identical procedure without any rGO under the contact metal. The complete device fabrication procedure is depicted in Figure 1a−f. The thicknesses of the thick, moderately thick, and very thin rGO sheets are in the range of 7, 2.5, and 1.7 nm, respectively, as obtained by cross-sectional high-resolution transmission electron microscopy (HRTEM) images (Figure 2a−c). Different layers of the MOS gate stack (Si, SiO_2, rGO, Pt, and TiN) are clearly visible in Figure 2.

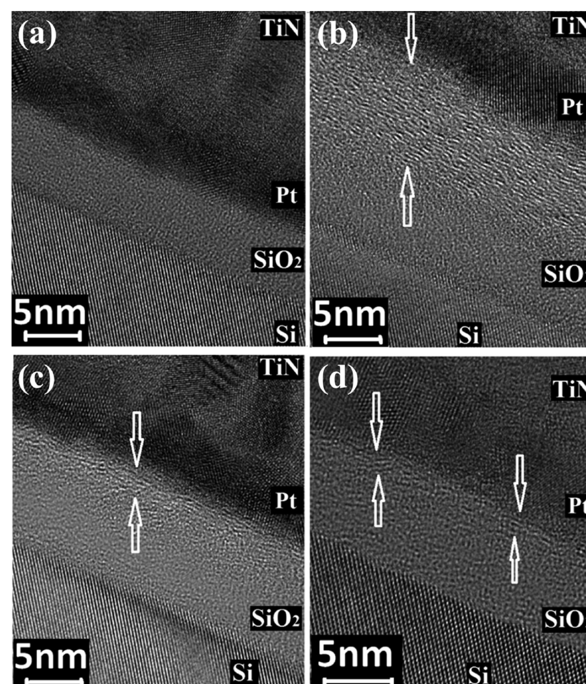

Figure 2. Cross-sectional HRTEM images of as-fabricated MOSCAPs: (a) without any rGO under Pt/TiN contact metal, (b) thick rGO under Pt/TiN contact metal, (c) moderately thick rGO under Pt/TiN contact metal, and (d) thin rGO under Pt/TiN contact metal.

Capacitance−voltage (CV) plots for rGO gate electrode devices with different capping metals (Pt/TiN, Ir/TiN, and Al/TiN) are shown in Figure 3. CV curves for the corresponding control sample (without rGO sheets) are also shown in the same figure. Flat band voltage (V_{FB}), obtained from the CV curves, is an important parameter that relates the gate electrode WF and amount of dielectric charges as per eq 1.[49]

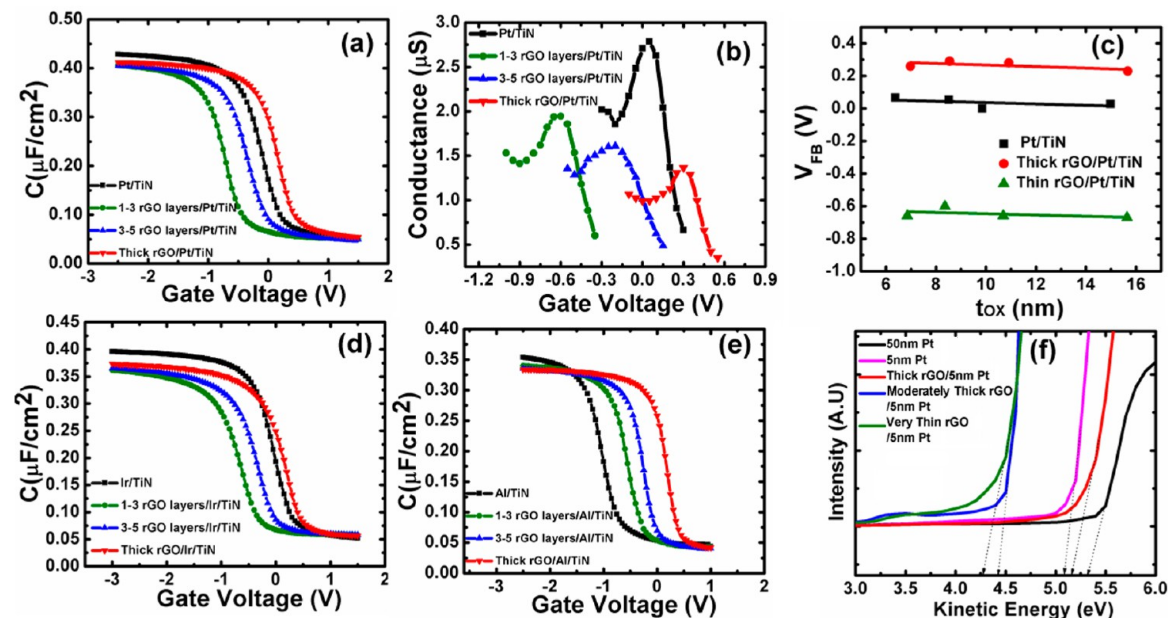

Figure 3. Panels (a)−(c) are the CV, GV, and V_{FB} vs t_{OX} plots of MOSCAPs with different thicknesses of rGO under Pt/TiN contact metal, respectively. (d, e) CV curves of MOSCAPs with different thicknesses of rGO under Ir/TiN and Al/TiN contact metals, respectively. (f) UPS spectra for 50 nm thick Pt film on SiO_2, 5 nm thick Pt film on SiO_2, and rGO with different thicknesses on SiO_2 with 5 nm of Pt deposited on it. Intersection of the dotted line with the arrow on the x axis gives the WF for different materials. UPS spectra in the entire measurement range are given as Figure S1 of the Supporting Information.

$$V_{FB} = \Phi_{ms} - \frac{Q_f + Q_{it}}{C_{OX}} = \Phi_{ms} - \frac{(Q_f + Q_{it})t_{OX}}{\varepsilon_0 \varepsilon_{OX}} \quad (1)$$

where

$$\Phi_{ms} = \Phi_m - \Phi_s \quad (2)$$

Here, Φ_m and Φ_s are the WFs of the metal and semiconductor (Si), respectively, Q_f is the fixed oxide charge per unit area in the SiO_2, Q_{it} is the charge per unit area at the interface of Si and SiO_2 at the flat band condition, C_{OX} is the oxide capacitance per unit area, ε_0 is the absolute permittivity of free space, ε_{OX} is the relative permittivity of the SiO_2, and t_{OX} is the thickness of SiO_2 calculated from the CV data.

From the minimum capacitance value (C_{min}) of the CV plot, the doping concentration of the semiconductor substrate is calculated as 1.5×10^{16} cm^{-3}, which, in turn, gives the semiconductor WF as 4.96 eV.[49] The flat band voltage for the $Si/SiO_2/Pt/TiN$ stack is 0.05 V, whereas it decreases to −0.6 and −0.2 V for very thin and moderately thin rGO sheets, respectively, and again increases to 0.29 V for thick rGO layers below the Pt/TiN contact metal. Equation 1 implies that the shift in flat band voltage can have contributions from charges in the oxide and the interface. To accurately determine the WF of a gate electrode in an MOS system, the contributions of the charge should be properly taken into account. Estimation of the oxide charges becomes even more important in the present study as the processing of rGO, especially its integration in the gate stack of an MOS structure could potentially introduce charges in the gate dielectric. In the present study, SiO_2 is chosen as a gate dielectric as it is the most widely explored dielectric in CMOS industry and forms an excellent interface with underlying silicon with minimum oxide charges. Moreover, all the charges in the SiO_2 reside close to the $Si-SiO_2$ interface,[49] and hence, the impact of these charges on the electrostatics of the graphene layers due to corresponding image charges would be minimal. In high-κ dielectrics, the charges in the dielectric are reported to be present in the central region of the dielectric or close to the top gate electrode.[50−52] These charges may substantially affect the charge distribution in the graphene and hence the electronic properties of graphene deposited on high-κ dielectrics. A thickness series experiment is commonly performed to separate the contributions of oxide charges and Φ_{ms} in the flat band voltage shift of MOS devices.[41,49] In this technique, MOS devices are fabricated with different thicknesses of the dielectric, and the flat band voltage is plotted as a function of the dielectric thickness as per eq 1. Here, it is assumed that the charges in the dielectric are independent of thickness and that the charges are at or near the interface between Si and SiO_2. The intercept of the linear fit of the data on the V_{FB} axis gives the WF difference between silicon and the gate electrode. The slope of the plot can be used to determine the oxide charges. The goodness of the fit is a test of the assumptions stated above.

To extract the value of WF of various thicknesses of rGO under contact metal, a thickness series experiment with four SiO_2 thicknesses (6.3, 8.5, 10, and 15 nm) has been performed. The flat band voltage vs t_{OX} data obtained from these experiments is plotted in Figure 3c. WF of Pt/TiN, very thin rGO/Pt/TiN, and thick rGO/Pt/TiN gate electrodes, extracted using eq 1, are 5.04, 4.35, and 5.28 eV, respectively. This shows that the WF of the gate electrode can be varied from 4.35 to 5.28 eV by varying the rGO thickness under Pt/TiN contact metal, as shown in the CV plot of Figure 3a. Total oxide charge densities, calculated using the slope of the V_{FB} vs t_{OX} plot and eq 1, are 9×10^{10}, 8.4×10^{10}, and 1×10^{11} cm^{-2} for Pt/TiN, thin rGO/Pt/TiN, and thick rGO/Pt/TiN gate electrodes, respectively.

In the conductance vs gate voltage (GV) plot of a MOS structure, the conductance peak (G_{Peak}) occurs close to the flat

band voltage,[49] and hence, the variation in the flat band voltage with different rGO thicknesses under Pt/TiN contact metal can also be verified by noting the position of conductance peak, as shown in Figure 3b. The G_{Peak} position shifts towards positive gate voltage from a value of −0.61 V for very thin rGO to 0.3 V for thick rGO, which is consistent with the flat band voltage values, obtained from the CV curves. Decreasing height of the conductance peak in GV plot signifies the reduced interface state density at the gate dielectric/semiconductor interface.[49] rGO, because of its superior mechanical properties, protects the gate dielectric from any plasma damage during top metal deposition (by sputtering in the present study), which results in an improved gate dielectric/semiconductor interface for rGO gate electrode devices.

The results of bidirectional (+ve as well as −ve) modulation of V_{FB} (and hence the gate electrode WF) are also obtained with rGO sheets under Ir/TiN contact metal. For calculating the WF of different rGO thicknesses under Ir/TiN contact metal, V_{FB} shift is directly equated to the Φ_{ms}. Here, it is assumed that the amount of oxide charges for Ir/TiN contact metal devices would be same as that for Pt/TiN contact metal as all the devices were processed under identical process conditions. These oxide charges would shift the V_{FB} by only ~0.04 V for Ir/TiN and rGO/Ir/TiN gate electrode devices for a 10 nm SiO_2 thickness. Hence, the assumption of neglecting the contribution of oxide charges to the flat band voltage is justified. WF values for different rGO thicknesses under Ir/TiN contact metal are 5.06 eV for no rGO and 4.4, 4.7, and 5.21 eV for very thin, moderately thick, and thick rGO layers, respectively. We have also carried out the same CV analysis with Al, which has a low WF value. With Al/TiN contact metal, a minimum WF of 4.46 eV with very thin rGO layers and a maximum WF of 5.16 eV for very thick rGO layers are obtained.

The difference in the WF values for thin rGO layers under different capping metals (Pt, Ir, Al) lies only within 0.12 eV. The spread in the data is similar for thick rGO sheets. This observation suggests that the flat band voltage (and hence the WF of gate electrode) is determined mainly by the rGO thickness, and the capping metals used in this work do not play any significant role in it. A possible explanation for this is discussed later in this paper. It is worth discussing here that, in the present case, the maximum WF difference (low value to high value) for thin and thick rGO is about 0.9 eV with Pt/TiN metal, whereas, for TiN metal only, the corresponding difference was 0.5 eV.[42] This difference can be due to the fact that, in the present work, the metals Pt, Ir, and Al are pure metals and are deposited by sputtering in pure Ar plasma, whereas the TiN metal was deposited in a reactive environment in the presence of N_2 and Ar plasma. Metals like Pt, Ir, and Al physisorb on Gr and thus may not affect the Gr properties.[36] However, the interaction of TiN with Gr, especially for TiN deposited by reactive sputtering, is not clear. We anticipate that the metal deposition conditions or the different interactions of TiN with rGO play some role in this.

The trend of WF variation of rGO thickness under Pt metal was also verified by ultraviolet photoelectron spectroscopy (UPS). For UPS analysis, rGO with different thicknesses were deposited on 4 nm of SiO_2 and a 5 nm Pt was deposited by sputtering on top of them. Pt thickness has been deliberately limited to 5 nm for UPS analysis as the energy of the photoelectrons is very low and usually very thin films are deposited for WF measurements by UPS.[53] A thick Pt (50 nm) sample on SiO_2 is also prepared for reference. UPS spectra are collected using a Thermo VG Scientific Multilab 2000 photoelectron spectrometer, which is equipped with a high photon flux He gas discharge source (modes: HeI 21.2 eV and HeII at 40.8 eV). UPS spectra support the thickness-dependent WF of the rGO/Pt system (Figure 3f). WF values obtained by CV measurements for different rGO thicknesses with different contact metals and by UPS measurements for the rGO/Pt system are plotted in Figure 4. Various values of the WF are summarized in Table S1 of the Supporting Information. In the present study, WF values by UPS measurements are lower than those obtained by CV measurements. The UPS technique is known to detect the lower limit of the WF of a system,[54] and hence, WF values obtained by UPS measurements are, in general, lower than the standard WF values.[54,55] Even though the WF values obtained from the two methods differ marginally, the trend of WF shift with varying the thickness of rGO under Pt metal is the same in both the measurement techniques.

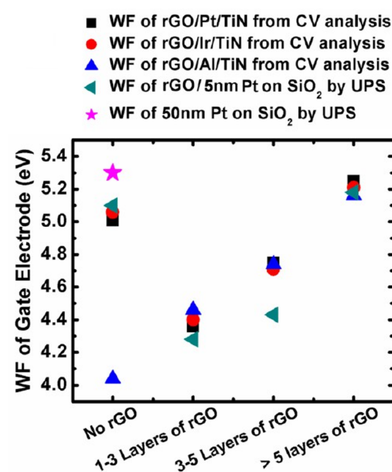

Figure 4. Modulation of the gate electrode WF with different numbers of rGO sheets under Pt/TiN, Ir/TiN, and Al/TiN capping metals. For comparison, WF values obtained from UPS analysis for rGO/5 nm Pt on SiO_2 and 50 nm Pt on SiO_2 are also plotted in the same figure.

Thermal stability of the different techniques adopted for WF modulation in CMOS technology is an important consideration.[30,56] Hence, we also examined the thermal stability of the WF values as obtained with the technique proposed above. Test the thermal stability of the rGO/Pt/TiN gate electrode, MOSCAPs were subjected to rapid thermal annealing in nitrogen ambient for temperatures ranging from 400 to 950 °C for 5 s each. The same sample from each split in the rGO thickness was subjected to an anneal−electrical measurement−anneal−electrical measurement...sequence, and the obtained results are shown in Figure 5a. Flat band voltage values of the Pt/TiN and rGO/Pt/TiN gate electrode devices remain stable till an annealing temperature of 800 °C. After 800 °C annealing, flat band voltage changes only by 0.06 and by 0.02 V for thin and thick rGO/Pt/TiN gate electrode devices, respectively. However, after 900 °C thermal annealing, flat band voltage of thin rGO/Pt/TiN devices increases significantly and approaches that of Pt/TiN electrode devices, while the flat band voltage of thick rGO/Pt/TiN MOSCAPs remains almost stable to its initial value of 0.26 V.

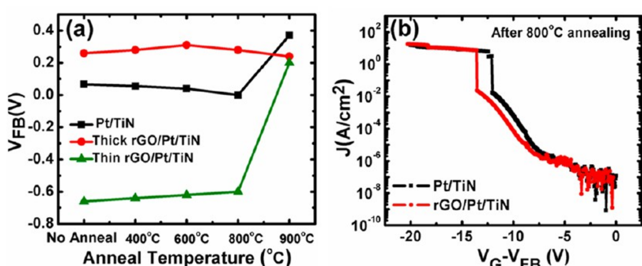

Figure 5. (a) Variation in the flat band voltage with annealing temperature for thick and thin rGO under Pt/TiN contact metal. (b) Comparison of breakdown characteristics for Si/SiO_2/PtTiN and Si/SiO_2/thick rGO/PtTiN after 800 °C annealing step.

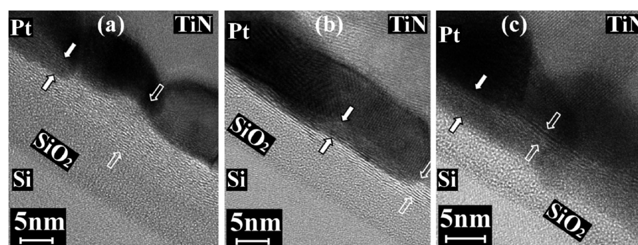

Figure 6. Cross-sectional HRTEM images of Si/SiO_2/rGO/Pt/TiN stack after thermal annealing at 900 °C for 5 s in N_2 ambient: (a) for thick rGO, (b) for moderately thick rGO, and (c) for very thin rGO. Hollow arrows demarcate the rGO, whereas solid arrows indicate the region of Pt diffusion in rGO/SiO_2. For thick and moderately thick rGO (a and b), Pt could not cross the full rGO thickness, whereas, for very thin rGO, Pt passes through the rGO and reacts with SiO_2.

To investigate the cause of this V_{FB} change after high-temperature processing, we performed cross-sectional HRTEM analysis of the sample annealed at 900 °C. High-temperature (900 °C) thermal annealing causes the Pt to diffuse through the rGO sheets, as shown in Figure 6. Low-magnification TEM images of rGO/Pt/TiN devices before and after thermal annealing are shown in Figure S2 of the Supporting Information. For thick and moderately thick rGO (Figure 6a,b), Pt could not pass through the rGO sheets completely, whereas, for very thin rGO (Figure 6c), Pt diffuses entirely through the rGO sheets and reacts with the SiO_2. As the Pt could not reach to the SiO_2 dielectric after annealing for the devices having thick rGO under Pt metal, the V_{FB} for these devices remains stable even after 900 °C annealing. V_{FB} for thin rGO devices approaches the V_{FB} of the SiO_2/Pt/TiN stack as the Pt is now in direct contact with SiO_2 after passing through the rGO sheets (Figure 6c). Diffusion of Pt and other metals into the graphitic network at higher temperatures is reported in other studies as well.[57,58] The CV curves for thin and thick rGO/Pt/TiN electrode devices after every thermal treatment are shown in Figure S3 of the Supporting Information. CV curves with rGO gate electrode devices remain steep even after 900 °C thermal annealing while a significant stretch out is observed in the CV curve for Pt/TiN gate electrode devices. This indicates the degradation of the gate dielectric in non-rGO gate electrode devices as a result of increasing annealing temperatures. This observation suggests that rGO gate electrode devices are more robust against any thermal treatment induced damage to the gate stack of the MOS devices. Figure 5b compares the breakdown behavior of Pt/TiN gate electrode devices with and without inclusion of rGO beneath it after the 800 °C thermal annealing step. rGO/Pt/TiN gate electrode devices result in less leakage and higher breakdown voltage values compared to only Pt/TiN electrode devices. This again indicates that the rGO gate electrode devices not only allow the tuning of WF but the quality of the gate dielectric also improves substantially.

A possible explanation for the experimental observations of the WF tuning reported above is as follows. The WF of the graphitic structure increases when the graphene layers increase from monolayer to multilayers as measured by different techniques, such as photoelectron spectroscopy and Kelvin probe force microscopy (KFM) methods.[31,32,38] Further, in a very recent theoretical study,[59] WF of the rGO is calculated using molecular dynamics simulations and density functional theory. This theoretical study reports that the WF of rGO increases with increasing oxygen concentration in the different groups, such as carbonyl, hydroxyl, and epoxy, attached to it. A range of WF values with different oxygen concentrations, i.e., 4.4−6.8 eV for the carbonyl group, 4.35−5.6 eV for the epoxy group, and 4.25−4.95 eV for the hydroxyl group, are reported. WF values obtained in our experiments (minimum of 4.35 eV for very thin rGO and maximum of 5.28 eV for thick rGO) are well within the range of these theoretical WF values. When the thermal reduction of GO is performed, thin GO can be expected to reduce more readily and loose its oxygen faster as compared to that of the thick GO . In multilayer GO, the layers below the top layers can be expected to reduce less effectively. Hence, the oxygen concentration would increase from thin rGO to thick rGO. To confirm this hypothesis, FTIR and XPS analyses are performed on different thicknesses of GO sheets before and after thermal reduction. Peaks corresponding to different functional groups, viz. hydroxyl (C−OH), epoxide (C−O−C), carboxyl (COOH), and ketonic (C═O), attached to the GO are marked in FTIR spectra shown in Figure 7a,b.[60] For very thin GO, after thermal reduction, the peak heights corresponding to different functional groups are almost negligible compared to those for moderately thick and very thick rGO. Slightly slow reduction of peak height for ketonic (C═O) and carboxyal groups (COOH) for moderately thick and very thick rGO is due to the high binding energy of oxygen with these functional groups.[60] This FTIR analysis clearly indicates that, under identical reduction conditions, removal of different functional groups depends on the GO thickness. As a result, oxygen concentration would be low in very thin rGO sheets (due to efficient removal of different functional groups) and would increase with rGO thickness.

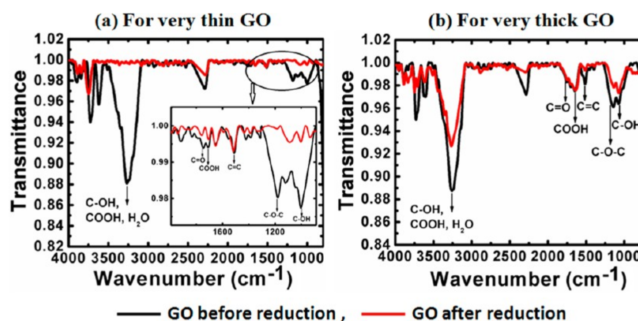

Figure 7. FTIR spectra (a) for very thin GO sheets and (b) for very thick GO sheets before and after thermal reduction of GO at 550 °C for 1 h in Ar ambient. Peaks corresponding to different functional groups attached to GO are assigned as per ref 60.

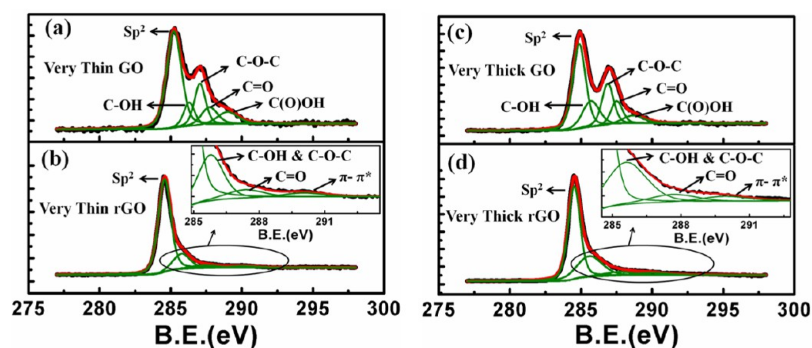

Figure 8. (a, b) XPS spectra of very thin GO before and after thermal reduction (rGO), respectively. (c, d) XPS spectra of very thick GO before and after thermal reduction (rGO), respectively.

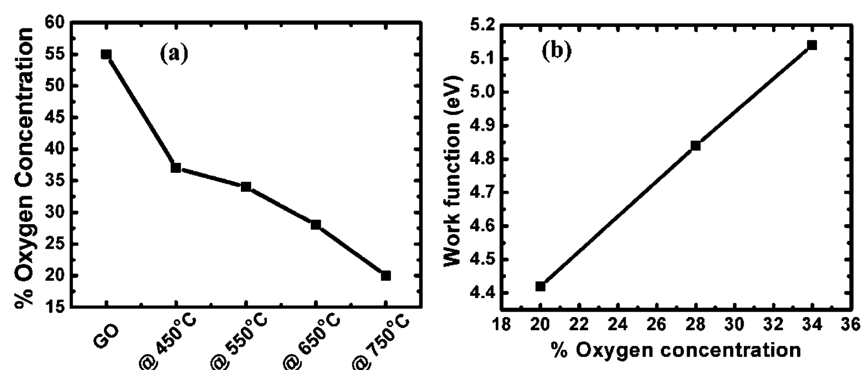

Figure 9. (a) Percent oxygen concentration of the thick rGO sheets with thermal reduction at different temperatures. (b) WF of the thick rGO sheets, with different oxygen concentrations, obtained from CV data.

To quantify the oxygen concentration in different thicknesses of rGO layers, XPS analysis is performed for very thin and thick GO sheets on the Si/SiO_2 substrate before and after thermal reduction. The XPS spectra of the C 1s peak are shown in Figure 8a–d. Peaks corresponding to different functional groups are marked in Figure 8a–d.[61–63] For GO (Figure 8a,c), the peak at a binding energy of about 284.8–285.1 eV is assigned to sp^2 carbon–carbon (C=C/C–C) bonds, whereas the peaks at 285.76, 286.78, 287.55, and 288.81 eV are assigned to C–OH, C–O–C, C=O, and COOH groups, respectively. After the thermal reduction, peak positions slightly decrease to lower binding energies, which is consistent with that reported in other studies.[61] After the thermal reduction, peaks corresponding to C–OH and C–O–C in very thin and thick rGO cannot be deconvoluted and are assigned as a single peak at 285.70 eV. Figure 8a–d clearly demonstrates that peaks corresponding to different oxygen-containing functional groups decrease faster for very thin rGO sheets as compared to those in very thick rGO sheets. Oxygen concentration in GO and rGO sheets is obtained after dividing the area of all peaks corresponding to oxygen-containing functional groups to the total area of the C 1s peak. In very thin and very thick GO (Figure 8a,c), O_2 concentration is about 46% and 55%, respectively, while the corresponding O_2 concentration after thermal reduction is about 22% and 37% for very thin and very thick GO sheets (Figure 8b,d). This analysis clearly reveals that thick rGO sheets, after identical reduction conditions, contain higher amounts of O_2 concentration. This variation in oxygen concentration, according to ref 59, would cause the WF of the rGO layers to vary from a low value to a high value. The observed WF modulation in the present study can be attributed to the combined effect of the two factors, namely, a thickness-dependent WF and the oxygen-defect-dependent WF.

Reduced GO with different oxygen concentrations can also be obtained by controlling the extent of the reduction for the same thickness of GO. Thick GO was reduced at different temperatures ranging from 450 to 750 °C for a duration of 1 h, and the MOSCAPs were fabricated with rGO under the Al gate electrode. Thick GO layers were chosen to exclude the contribution of layer-dependent WF. XPS spectra of thick GO layers reduced at different temperatures are shown in Figure S4a–d of the Supporting Information, and the remnant oxygen concentration in the rGO sheets versus their WF under Al contact metal is plotted in Figure 9. As the reduction temperature increases, peak heights corresponding to different oxygen-containing functional groups and hence oxygen concentration decrease. For GO, the oxygen concentration is about 55 %, while it decreases to 37, 34, 28, and 20% after thermal treatment at 450, 550, 650, and 750 °C temperatures, respectively. This reduction in the oxygen concentration causes the WF of the rGO/Al stack to decrease from 5.14 to 4.42 eV for a reduction in temperatures from 550 to 750 °C, as shown in Figure 9. This experiment clearly demonstrates that oxygen concentration plays a significant role in determining the reduced graphene oxide work function.

Here, the effect of contacting metal on the WF of different rGO thicknesses is worth discussing. Impact of metal contacts on the reduced graphene oxide has not been explored much. On the other hand, a significant work has been done on the impact of metal contact on graphene.[34–37,64,65] However, the theoretical and experimental studies for the WF of graphene beneath a metal differ significantly. A simple charge transfer

model based on the difference in the Fermi levels of the graphene and the metal was proposed by Chan et al.[64] Further, Giovannetti et al. added an interfacial dipole to this charge transfer model.[34] On the basis of this model, p-type and n-type doping of the graphene is predicted by Pt and Cu metals, respectively. However, Pi et al.[35] experimentally reported n-type doping of the graphene by Pt metal, thus contradicting the theoretical predictions of ref 34. Similarly, theoretical calculations for Au on graphene[64] suggest an increase in graphene WF. This, however, contradicts the observed WF value of 4.64 eV for monolayer graphene under Au and Pd contacts.[41]

These discrepancies in the observed experimental results and theoretical models can be explained based on the facts that the charge transfer may be a secondary effect and the nature of chemical interaction between metal and the graphene (chemisorption or physisorption) determines the graphene WF, as discussed by Gong et al.[36] It is well-understood that metals such as Pt, Al, and Ir interact weakly with graphene, and hence, the electronic nature of the graphene is preserved under these metals.[36,66] The possibility of charge transfer between such metals and graphene is not ruled out in these studies. However, the results of the present study suggest that the level of the charge transfer between rGO and these metals may not be very significant, and hence, the rGO preserves its electronic nature under the metals that essentially physisorb on it. Further, in an MOS capacitor, the flat band voltage is decided by the graphene/dielectric interface, in contrast to other structures used in most of the reported experimental studies. The contact metal may influence the WF of this interface by the penetration of the electron wave functions from the metal through the graphene. The metals used in this study (Pt, Ir, Al) are physisorbed on graphene with a larger distance from the graphene plane than that of metals that are chemisorbed.[34,67] In the present study, the WF of the MOS system is most likely determined by the rGO/dielectric interface than the capping metal due to the limited influence of these metals (Pt, Ir, Al) on the electronic structure of rGO.

CONCLUSIONS

It is demonstrated that the WF of the rGO/metal gate electrode in an MOS structure can be tuned from a low value (n-type metal) to a high value (p-type metal) by controlling the oxygen concentration in the rGO sheets under different contact metals such as Pt, Ir, and Al. Oxygen concentration in the rGO sheets can be varied either by varying the thickness of the rGO sheets or by performing the reduction process at different temperatures. This is a very important methodology to control the WF of rGO sheets by controlling the inherent property of the graphene oxide. The proposed technique is stable up to a 800 °C thermal annealing temperature. Postannealing X-HRTEM analysis of the samples reveals that the diffusion of metal through rGO layers at higher temperatures is the main cause of WF instability. The results of the present study are not limited to MOS technology and can be extended to other technologies such as OLEDs and OPVs where graphene is proposed to be used as conducting electrodes. However, a tight control over the placement of a known number of graphene layers with a controlled amount of oxygen concentration is essential and has to be developed from an industrial application point of view.

ASSOCIATED CONTENT

Supporting Information

Synthesis of graphene oxide and details of the device fabrication procedure are given in the Supporting Information. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Novoselov, K. S.; Falko, V. I.; Colombo, L.; Gellert, P. R.; Schwab, M. G.; Kim, K. *Nature* **2012**, *490*, 192.

(2) Xia, F.; Mueller, T.; Lin, Y. M.; Garcia, A. V.; Avouris, P. *Nat. Nanotechnol.* **2009**, *4*, 839.

(3) Liao, L.; Bai, J.; Cheng, R.; Lin, Y. C.; Jiang, S.; Qu, Y.; Huang, Y.; Duan, X. *Nano Lett.* **2009**, *10*, 3430.

(4) Badmaev, A.; Che, Y.; Li, Z.; Wang, C.; Zhou, C. *ACS Nano* **2012**, *6*, 3371.

(5) Liu, M.; Yin, X.; Avila, E. U.; Geng, B.; Zentgraf, T.; Ju, L.; Wang, F.; Zhang, X. *Nature* **2011**, *474*, 64.

(6) Han, T. H.; Lee, Y.; Choi, M. R.; Woo, S. H.; Bae, S. H.; Hong, R. H.; Ahn, J. H.; Lee, T. W. *Nat. Photonics* **2012**, *6*, 105.

(7) Sun, T.; Wang, Z. L.; Shi, Z. J.; Ran, G. Z.; Xu, W. J. *Appl. Phys. Lett.* **2010**, *96*, 133301.

(8) Jo, G.; Na, S. In.; Oh, S. H.; Lee, S.; Kim, T. S.; Wang, G.; Choe, M.; Park, W.; Yoon, J.; Kim, D. Yu.; et al. *Appl. Phys. Lett.* **2010**, *97*, 213310.

(9) Hwang, J. O.; Park, J. S.; Choi, D. S.; Kim, J. Y.; Lee, S. H.; Lee, K. E.; Kim, Y. H.; Song, M. H.; Yoo, S.; Kim, S. O. *ACS Nano* **2010**, *6*, 159.

(10) Park, H.; Brown, P. R.; Bulovic, V.; Kong, K. *Nano Lett.* **2012**, *12*, 133.

(11) Ou, X.; Jiang, L.; Chen, P.; Zhu, M.; Hu, W.; Liu, M.; Zhu, J.; Ju, H. *Adv. Funct. Mater.* **2012**, *22*, 2422.

(12) Lee, W. H.; Park, J.; Sim, S. H.; Lim, S.; Kim, K. S.; Hong, B. H.; Cho, K. *J. Am. Chem. Soc.* **2011**, *133*, 4447.

(13) Wu, J.; Becerril, H. A.; Bao, Z.; Liu, Z.; Chen, Y. *Appl. Phys. Lett.* **2008**, *92*, 263302.

(14) Kwon, K. C.; Choi, K. S.; Kim, S. Y. *Adv. Funct. Mater.* **2012**, *22*, 4724.

(15) Hwang, J.; Choi, H. K.; Moon, J.; Kim, T. Y.; Shin, J. W.; Joo, C. W.; Han, J. H.; Cho, D. H.; Huh, J. W.; Choi, S. Y.; Lee, J. I.; Chu, H. Y. *Appl. Phys. Lett.* **2012**, *100*, 133304.

(16) Kwon, K. C.; Dong, W. J.; Jung, G. H.; Ham, J.; Lee, J. L.; Kim, S. Y. *Sol. Energy Mater. Sol. Cells* **2013**, *109*, 148.

(17) Cox, M.; Jia, Z.; Gorodetsky, A.; Kim, B.; Kim, K. S.; Jia, Z.; Kim, P.; Nuckolls, C.; Kymissis, I. *Appl. Phys. Lett.* **2011**, *98*, 123303.

(18) Kwon, K. C.; Choi, K. S. *J. Phys. Chem. C* **2012**, *116*, 26586.

(19) International Technology Roadmap for Semiconductors, 2010 Edition. Available online at www.itrs.net.

(20) Yeo, Y. C.; Lu, Q.; Ranade, P.; Takeuchi, H.; Yang, K. J.; Polishchuk, I.; King, T. J.; Hu, C.; Song, S. C.; Luan, H. F. *IEEE Electron Device Lett.* **2001**, *22*, 227.
(21) Hsu, P. F.; Hou, Y. T.; Yen, F. Y.; Chang, V. S.; Lim, P. S.; Hung, C. L.; Yao, L. G.; Jiang, J. C.; Lin, H. J.; Chiou, J. M.; et al. *Symp. VLSI Techol., Dig. Tech. Pap.* **2006**, 11.
(22) Mistry, K.; Allen, C.; Auth, C.; Beattie, B.; Bergstrom, D.; Bost, M.; Brazier, M.; Buehler, M.; Cappellani, A.; Chau, R. *IEDM Tech. Dig.* **2007**, 247.
(23) Misra, V.; Zhang, H.; Lazar, H. *IEEE Electron Device Lett.* **2002**, *23*, 354.
(24) Park, D. G.; Cha, T. H.; Lim, K. Y.; Cho, H. J.; Kim, T. K.; Jang, S. A.; Suh, Y. S.; Misra, V.; Yeo, In. S.; Roh, J. S. *IEDM Tech. Dig.* **2001**, 671.
(25) Polishchuk, I.; Ranade, P.; King, T. J.; Hu, C. *IEEE Electron Device Lett.* **2002**, *23*, 200.
(26) Lin, R.; Lu, Q.; Ranade, P.; King, T. J.; Hu, C. *IEEE Electron Device Lett.* **2002**, *23*, 49.
(27) Jeon, I. S.; Lee, J.; Zhao, P.; Sivasubramani, P.; Oh, T.; Kim, H. J.; Cha, D.; Huang, G.; Kim, M. J.; Gnade, B. E.; Kim, J. *IEDM Tech. Dig.* **2004**, 303.
(28) Lin, C. T.; Ramin, M.; Pas, M.; Wise, R.; Fang, Y. K.; Hsu, C. H.; Huang, Y. T.; Cheng, L. W.; Ma, M. *IEEE Electron Device Lett.* **2007**, *28*, 831.
(29) Kittl, J. A.; Lauwers, A.; Veloso, A.; Hoffmann, T.; Kubicek, S.; Niwa, M.; Vandal, M. J. H; Pawlak, M. A.; Brus, S.; Demeurisse, C. *IEEE Electron Device Lett.* **2007**, *27*, 966.
(30) Tsui, B. Y.; Huang, C. F. *IEEE Electron Device Lett.* **2003**, *24*, 153.
(31) Hibino, H.; Kageshima, H.; Kotsugi, M.; Maeda, F.; Guo, F. Z.; Watanabe, Y. *Phys. Rev. B* **2009**, *79*, 125437.
(32) Yu, Y. J.; Zhao, Y.; Ryu, S.; Brus, L. E.; Kim, K. S.; Kin, P. *Nano Lett.* **2009**, *9*, 3430.
(33) Park, J. K.; Song, S. M.; Mun, J. H.; Cho, B. J. *Nano Lett.* **2011**, *11*, 5383.
(34) Giovannetti, G.; Khomyakov, P. A.; Brocks, G.; Karpan, V. M.; Brink, J. V. D.; Kelly, P. J. *Phys. Rev. Lett.* **2008**, *101*, 026803.
(35) Pi, K.; McCreary, K. M.; Bao, W.; Han, W.; Chiang, Y. F.; Li, Y.; Tsai, S. W.; Lau, C. N.; Kawakami, R. K. *Phys. Rev. B* **2009**, *80*, 075406.
(36) Gong, C.; Lee, G.; Shan, B.; Vogel, E. M.; Wallace, R. M.; Cho, K. *J. Appl. Phys.* **2010**, *108*, 123711.
(37) Santos, J. E.; Peres, N. M. R.; Lopes dos Santos, J. M. B.; Neto, A. H. C. *Phys. Rev. B* **2011**, *84*, 085430.
(38) Zeigler, D.; Gava, P.; Guttinger, J.; Molitor, F.; Wirtz, L.; Lazzeri, M.; Saitta, A. M.; Stemmer, A.; Mauri, F.; Stampfer, C. *Phys. Rev. B* **2011**, *83*, 235434.
(39) Ihm, K.; Tim, J.; Lee, K. J.; Kwon, J. W.; Kang, T. H.; Chung, S.; Bae, S.; Kim, J. H.; Hong, B. H.; Yeom, G. Y. *Appl. Phys. Lett.* **2010**, *97*, 032113.
(40) Park, J. K.; Song, S. M.; Mun, J. H.; Cho, B. J. *Symp. VLSI Technol., Dig. Tech. Pap.* **2012**, 31.
(41) Song, S. M.; Park, J. K.; Sul, O. J.; Cho, B. J. *Nano Lett.* **2012**, *12*, 3887.
(42) Misra, A.; Waikar, M.; Gour, A.; Kalita, H.; Khare, M.; Aslam, M.; Kottantharayil, A. *Appl. Phys. Lett.* **2012**, *100*, 233506.
(43) Wang, X.; Zhi, L.; Mullen, K. *Nano Lett.* **2008**, *8*, 323.
(44) Park, S.; Ruoff, R. S. *Nat. Nanotechnol.* **2009**, *4*, 217.
(45) Wobkenberg, P. H.; Eda, G.; Leem, D.-S.; de Mello, J. C.; Bradly, D. D. C.; Chhowalla, M.; Anthopoulos, T. D. *Adv. Mater.* **2011**, *23*, 1558.
(46) Eda, G.; Lin, Y. Y.; Miller, S.; Chen, C. W.; Su, W. F.; Chhowalla, M. *Appl. Phys. Lett.* **2008**, *92*, 233305.
(47) Pang, S.; Tsao, H. N.; Feng, X.; Mullen, K. *Adv. Mater.* **2009**, *21*, 3488.
(48) Wu, J.; Agrawal, M.; Becerril, H. A.; Bao, Z.; Liu, Z.; Chen, Y.; Peumans, P. *ACS Nano* **2010**, *4*, 43.
(49) Nicollian, E. H.; Brews, J. R. In *MOS (Metal Oxide Semiconductor) Physics and Technology*; Wiley: New York, 1982; p 426.
(50) Zhang, J. F.; Zhao, C. Z.; Zahid, M. B.; Groeseneken, G.; Degraeve, R.; Gendt, S. D. *IEEE Electron Device Lett.* **2006**, *27*, 817.
(51) Felnhofer, D.; Gusev, E. P.; Jamison, P.; Buchanan, D. A. *Microelectron. Eng.* **2005**, *80*, 58.
(52) Xiong, H. D.; Heh, D.; Gurufinkel, M.; Li, Q.; Shapira, Y.; Richter, C.; Bersuker, G.; Choi, R.; Suehle, J. S. *Microelectron. Eng.* **2007**, *84*, 2230.
(53) Park, Y.; Choong, V.; Gao, Y.; Hsieh, B. R.; Tang, C. W. *Appl. Phys. Lett.* **1996**, *68*, 2699.
(54) Kim, J. S.; Lagel, B.; Moons, E.; Johansson, N.; Baikie, I. D.; Salaneck, W. R.; Friend, R. H.; Cacialli, F. *Synth. Met.* **2000**, *111−112*, 311.
(55) Gutmann, S.; Conrad, M.; Wolak, M. A.; Beerbom, M. M.; Schlaf, R. *J. Appl. Phys.* **2012**, *111*, 123710.
(56) Yu, H. Y.; Ren, C.; Yeo, Y. C.; Kang, J. F.; Wang, X. P.; Ma, H. H. H.; Li, M. Fu.; Chan, D. S. H.; Kwog, D. L. *IEEE Electron Device Lett.* **2004**, *25*, 337.
(57) Gan, Y.; Sun, L.; Banhart, F. *Small* **2008**, *4*, 587.
(58) Kim, H. Y.; Lee, C.; Kim, J.; Ren, F.; Pearton, S. J. *J. Vac. Sci. Technol., B* **2012**, *30*, 030602.
(59) Kumar, P. V.; Bernardi, M.; Grossman, J. C. *ACS Nano* **2013**, *2*, 1638.
(60) Acik, M.; Lee, G.; Mattevi, C.; Chhowalla, M.; Cho, K.; Chabal, Y.J. *Nat. Mater.* **2010**, *9*, 840−845.
(61) Ganguly, A.; Sharma, S.; Papakonstantinou, P.; Hamilton, J. *J. Phys. Chem. C* **2011**, *115*, 17009.
(62) Yang, D.; Velamakanni, A.; Bozoklu, Gu. L.; Park, S.; Stoller, M.; Piner, R. D.; Stankovich, S.; Jung, I.; Field, D. A.; Ventrice, C. A. J.; Ruoff, R. S. *Carbon* **2009**, *47*, 145.
(63) Lee, S. W.; Mattevi, C.; Chhowalla, M.; Sankaram, R. M. *J. Phys. Chem. Lett.* **2012**, *3*, 772.
(64) Chan, K. T.; Neaton, J. B.; Cohen, M. L. *Phys. Rev. B* **2008**, *77*, 235430.
(65) Xia, F.; Pereveinos, V.; Lin, Y. M.; Wu, Y.; Avouris, P. *Nat. Nanotechnol.* **2011**, *6*, 179.
(66) Khomyakov, P. A.; Giovannetti, G.; Rusu, P. C.; Brocks, G.; Brink, J. V. D.; Kelly, P. J. *Phys. Rev. B* **2009**, *79*, 195425.
(67) Vanin, M.; Mortensen, J. J.; Kelkkanen, A. K.; Garcia-Lastra, J. M.; Thygesen, K. S.; Jacobsen, K. W. *Phys. Rev. B* **2010**, *81*, 081408(R).